REMARKS

Reexamination and reconsideration of the present application are requested.

Applicants wish to thank the Examiner for the courtesy of an Examiner Interview with Applicants' attorney on 21 January 2003 to discuss this application.

Applicants have amended claims 1, 9, 12 and 15 and canceled claims 3 and 17. Accordingly, claims 1, 2, 4, 5, 7-16, and 18-20 remain pending in the application.

Claim 1

As amended, the method of claim 1 includes a combination of features wherein: the plate electrode is formed of one selected from the group consisting of Pt, Ru, Ir, IrO_2, RuO_2, $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, and an alloy containing Ir; the plate electrode is formed directly on the high dielectric layer; and first and second annealings are performed, the first annealing being in an inert environment at a first (higher) temperature, and the second annealing being in an oxygen environment as a second (lower) temperature.

Such a combination of features is not disclosed or suggested by any combination of the cited prior art references.

As taught in the specification, in the prior art "a barrier layer must be formed between the noble metal electrode and the high dielectric layer" (page 2, lines 7-8). However, the present inventors have discovered that recited first annealing (in an inert environment at a higher temperature) and second annealing (in an oxygen environment at a lower temperature) allow a noble-metal-based plate electrode to be formed directly on the high dielectric layer without any intervening barrier layer.

Meanwhile, Al-Shareef discloses a process wherein a barrier layer 28 is formed on the high dielectric layer 26. Subsequently, a polysilicon layer 230 is formed on the barrier layer 28. That is, Al-Shareef fails to teach the formation of a noble-metal-based plate electrode directly on the high dielectric layer.

Accordingly, it is respectfully submitted that claim 1 is patentable over Al-Shareef alone or in combination with Ping. Claims 2, 4, 5, 8, 10, 11, 13 and 14, dependent from claim 1, are deemed allowable for at least these same reasons.

Claims 9, 15, 16, and 18-20

Similarly to claim 1, the methods of claims 9 and 15 each include a combination of features wherein: the plate electrode is formed of one selected from the group consisting of Pt, Ru, Ir, IrO_2, RuO_2, $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, and an alloy containing Ir; the plate electrode is formed directly on the high dielectric layer; and first and second annealings are performed, the first annealing being in an inert environment at a first (higher) temperature, and the second annealing being in an oxygen environment as a second (lower) temperature.

As explained above, such a combination of features is not disclosed or suggested by any combination of the cited prior art references.

Moreover, in the method of claim 9, both the first and second annealings are performed after the plate electrode is formed. Such a feature is not taught by the cited prior art references, nor, it is respectfully submitted, would one reading the prior art

references be motivated to modify their teachings to perform both the first and second annealings after the plate electrode is formed.

The Office Action stated that "Al-Shareef anticipated performing the anneals after the formation of the plate electrode, but concluded that such a strategy was undesirable for the reasons disclosed by the reference. . . . The reference need not agree with applicant to have anticipated the claimed invention."

However, rather than anticipating the claimed invention, Al-Shareef specifically ***teaches away*** from the claimed method, teaching that the annealings are to be conducted "***prior to formation of ANY portion of the second capacitor electrode 32***" to minimize the risk of oxidation of the plate electrode 32 due to out-diffusion of oxygen from the high dielectric layer 26 (col. 5, lines 6-11). This was especially critical for Al-Shareef in so much as it teaches that the plate electrode is a polysilicon layer, not a noble-metal-based material as in the invention of claim 9.

M.P.E.P. § 2141.02 states that "PRIOR ART MUST BE CONSIDERED IN ITS ENTIRETY, INCLUDING DISCLOSURES THAT TEACH AWAY FROM THE CLAIMS" (emphasis in original text). For example, it was held that a reference teaching that a PTFE material should be stretched slowly ***taught away from*** a claimed process that included a step of rapidly stretching the PTFE material (M.P.E.P. § 2141.02 citing W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984)). So, in that case, the reference "anticipated performing [a rapid stretching of the PTFE material], but concluded that such a strategy was undesirable for the reasons disclosed by the

reference" (paraphrasing the Office Action). However, the courts concluded that the reference taught away from the claimed process and could not be used - or even combined with any other reference (see M.P.E.P. § 2145 - "*it is improper to combine references where the references teach away from their combination*") - to produce the claimed invention. Applicants respectfully submit that this is exactly the same case here with respect to Al-Shareef.

Meanwhile, even assuming arguendo that Wolf teaches that anneals occur after formation of the capacitor, it does not teach the recited first and second annealings under the specifically recited conditions of claim 9. Nor, as explained above, can it be combined with Al-Shareef that teaches away from the method of claim 9.

Accordingly, it is respectfully submitted that claim 9 is patentable over Al-Shareef alone or in combination with Azuma and Wolf. Claims 16 and 18-20, dependent from claim 15, are deemed allowable for at least these same reasons.

Claim 12

Similarly to claim 1, the method of claim 12 includes a combination of features wherein: the plate electrode is formed of one selected from the group consisting of Pt, Ru, Ir, IrO_2, RuO_2, $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, and an alloy containing Ir; the plate electrode is formed directly on the high dielectric layer; and first and second annealings are performed, the first annealing being in an inert environment at a first (higher) temperature, and the second annealing being in an oxygen environment as a second (lower) temperature.

As explained above, such a combination of features is not disclosed or suggested by any combination of the cited prior art references.

Furthermore, in the method of claim 12, both the first and second annealings are performed after the interdielectric layer is formed. Such a feature is not taught by the cited prior art references, nor, it is respectfully submitted, would one reading the prior art references be motivated to modify their teachings to perform both the first and second annealings after the interdielectric layer is formed.

As explained above, Al-Shareef specifically teaches away from the claimed method, teaching that the annealings are to be conducted prior to formation of any portion of the second capacitor electrode, and therefore necessarily prior to formation of the interdielectric layer.

Accordingly, it is respectfully submitted that claim 12 is patentable over Al-Shareef alone or in combination with Azuma and Wolf.

CONCLUSION

In view of the foregoing explanations, Applicant respectfully requests that the Examiner reconsider and reexamine the present application, allow claims 1, 2, 4, 5, 7-16, and 18-20, and pass the application to issue. In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Kenneth D. Springer (Reg. No. 39,843) at (703) 715-0870 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17, particularly extension of time fees.

Respectfully submitted,

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Version with Markings to Show Changes Made

In the Claims:

Claims 3 and 17 have been canceled.

Claims 1, 9, 12 and 15 have been amended as follows:

1. (Twice Amended) A method for manufacturing a capacitor of a semiconductor device, comprising:

forming a storage electrode over a semiconductor substrate;

forming a high dielectric layer over the storage electrode;

forming a plate electrode [over] directly on the high dielectric layer;

performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature; and

performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature in an oxygen environment,

the first and second post-annealings being performed in-situ,

wherein the plate electrode is formed of one selected from the group consisting of Pt, Ru, Ir, IrO_2, RuO_2, $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, and an alloy containing Ir.

9. (Three Times Amended) A method for manufacturing a capacitor of a semiconductor device, comprising:

forming a storage electrode over a semiconductor substrate;

forming a high dielectric layer over the storage electrode;

forming a plate electrode [over] directly on the high dielectric layer;

performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature; and

performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature in an oxygen environment,

the first and second post-annealings being performed after the forming of the plate electrode,

wherein the plate electrode is formed of one selected from the group consisting of Pt, Ru, Ir, IrO_2, RuO_2, $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, and an alloy containing Ir.

12. (Twice Amended) A method for manufacturing a capacitor of a semiconductor device, comprising:

forming a storage electrode over a semiconductor substrate;

forming a high dielectric layer over the storage electrode;

forming a plate electrode [over] directly on the high dielectric layer;

performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature;

performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature in an oxygen environment; and

forming an interdielectric layer over the plate electrode,

the first and second post-annealings being performed after the forming of the interdielectric layer,

wherein the plate electrode is formed of one selected from the group consisting of Pt, Ru, Ir, IrO_2, RuO_2, $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, and an alloy containing Ir.

15. (Twice Amended) A method for manufacturing a capacitor of a semiconductor device in which: a storage electrode;[,] a high dielectric layer;[,] a plate electrode formed directly on the high dielectric layer and comprising one selected from the group consisting of Pt, Ru, Ir, IrO_2, RuO_2, $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, and an alloy containing Ir;[,] and an interdielectric layer are sequentially formed on a semiconductor substrate, further comprising:

performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature; and

performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature in an oxygen environment,

the first and second post-annealings being performed after forming of the plate electrode.